

WHAT IS CLAIMED IS:

1. A jitter reducing apparatus, comprising:

an elastic store that stores data received from a synchronous digital hierarchy (SDH) network;

a pattern generator that controls a data read speed so the elastic store maintains a constant amount of stored data;

a modulation sequencer that generates signals representative of a digital signal wave having a constant period and amplitude; and

a phase level detector that controls the pattern generator using the digital signal wave.

2. The apparatus of claim 1, wherein the phase level detector controls the pattern generator using a difference value between the amount of stored data in the elastic store and an amount of data outputted from the elastic store, less a value of the digital signal wave.

3. The apparatus of claim 1, wherein the phase level detector is operated at time intervals upon receipt of the digital signal wave from the modulation sequencer.

4. The apparatus of claim 1, wherein the pattern generator performs a controlling operation of a pattern generation speed at regular time intervals.

5. The apparatus of claim 1, wherein the modulation sequencer is operated upon receipt of an 8KHz frame pulse and a 6.48MHz clock frequency.

6. The apparatus of claim 5, wherein the modulation sequencer generates the digital signal wave of which one period is 16 sections of the frame pulse and has a 500 Hz bandwidth.

7. The apparatus of claim 1, wherein the modulation sequencer outputs a mode-value signal indicative of an amplitude level of the digital signal wave and a mode-slope signal indicative of a positive and a negative direction of the digital signal wave.

8. The apparatus of claim 7, wherein the mode-slope signal controls a positive section or a negative section of the digital signal wave.

9. The apparatus of claim 7, wherein the mode-value signal repeats four signal values of 00,01,10, and 11.

10. The apparatus of claim 7, wherein the mode-value signal and the mode-slope signal implement a binary code signal with a high voltage level and a low voltage level.